

The Common Platform Technology: A New Model for Semiconductor Manufacturing

SKU: IN0703405WHT
Analyst: Jim McGregor
Jim.mcgregor@reedbusiness.com
+1.480.609.4554
January 5, 2007

Executive Summary

The cost of semiconductor manufacturing continues to climb and drive changes in the market. Not only have state-of-the-art 90nm and 65nm fabs now reached an average cost of nearly US \$5 billion, the cost of developing the process technology continues to rise with each generation. Likewise, the cost of manufacturing continues to increase. The cost of developing mask sets, which are unique to every product and usually every fab exceeds US\$1 million per set and is expected to continue to increase exponentially with each process node. These rising costs and other market dynamics have combined in the past to drive the separation between fabless semiconductor companies and foundry models that are predominant today.

Now, the same trends are shrinking the number of semiconductor companies with fabs and foundries to below 40. Many semiconductor manufacturers and foundries have turned to joint process technology development, which addresses one side of the cost equation. There are at least three major alliances aimed at developing advanced CMOS process technology—IBM's SOI Alliance, Crolles2 alliance, and the Advanced SoC Platform Corporation (ASPLA).

Chartered Semiconductor Manufacturing, IBM and Samsung have now developed a new model that addresses both the cost of fab capacity and process development, while providing a cohesive design ecosystem through what has been named Common Platform™ technology. They have extended their joint bulk CMOS development alliance to include joint manufacturing capability. The Common Platform technology partners have generated a number of new benefits for clients, including:

- Full product development, manufacturing, and product lifecycle support from three leaders in semiconductor design, process technology, and manufacturing
- Multi-sourcing a single design through GDSII compatibility to globally-diverse synchronized fabs for risk mitigation and/or upside support
- Choice of design enablement resources (libraries, IP, reference flows, EDA tools, and packaging), including a robust set of Design for Manufacturing (DFM) tools jointly supported by multiple tool vendors, design centers, and foundry partners
- Engineering services and support from three companies with expertise in every aspect of semiconductor design and manufacturing

The Common Platform technology alliance has established a new model for semiconductor design and manufacturing through a new level of collaboration amongst industry leaders. This new model is gaining tremendous momentum with at least fifteen design tool/EDA/IP partners joining to provide a comprehensive design ecosystem plus the industry leading packaging vendor, Amkor. In the latest report on fab synchronization, all three factories are centered on all 65nm Low Power device parameters within less than 5% deviation. The Microsoft Xbox 360 processor was a powerful proof point to demonstrate IBM and Chartered's fab synchronization and manufacturing capabilities. Subsequently QUALCOMM is leveraging the platform's benefits for 90nm production and beyond.

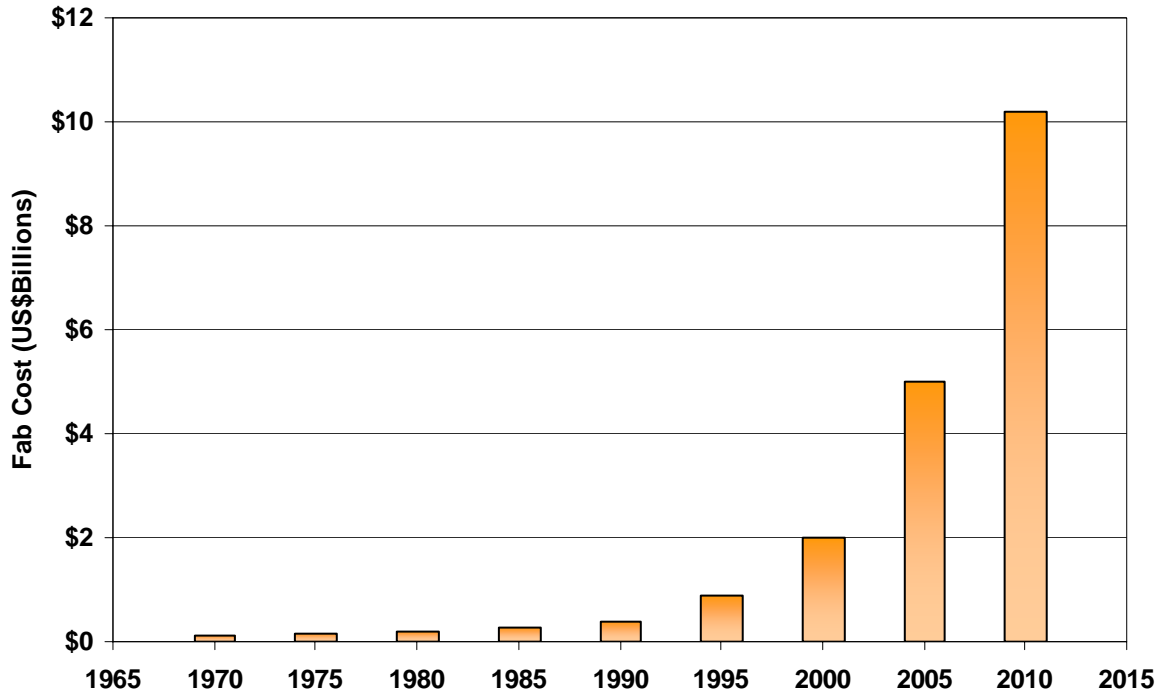
Table of Contents

| | | | |
|--|----|--|--------------------|
| Executive Summary..... | 1 | Chartered Semiconductor Manufacturing..... | 15 |
| Introduction..... | 3 | IBM..... | 15 |
| Evolution of the Semiconductor Business Model | 5 | Samsung..... | 16 |
| The Old Model..... | 5 | Risk Mitigation..... | 17 |
| The New Model..... | 5 | Different Equipment and Fab Automation Tools..... | 17 |
| The Client Value Proposition..... | 8 | Different Mask Sets..... | 17 |
| Manufacturing Capacity and Efficiency..... | 8 | Different Companies..... | 17 |
| Manufacturing Flexibility..... | 9 | Different Cultures..... | 18 |
| Unmatched Process Expertise..... | 10 | New Process Technologies..... | 18 |
| Increased Engineering Resources..... | 10 | Results in Action..... | 19 |
| Qualification and Packaging..... | 10 | A Leading Industry Trend..... | 20 |
| Common Resources..... | 11 | Conclusions..... | 22 |
| Ecosystem Development..... | 13 | List of Tables..... | 23 |
| The Partner Value Proposition..... | 14 | List of Figures..... | 23 |

Introduction

The cost of semiconductor manufacturing continues to climb and drive changes in the market. Not only have state-of-the-art 90nm and 65nm fabs now reached an average cost of nearly US\$5 billion (Figure 1), but the cost of developing the process technology continues to rise with each generation.

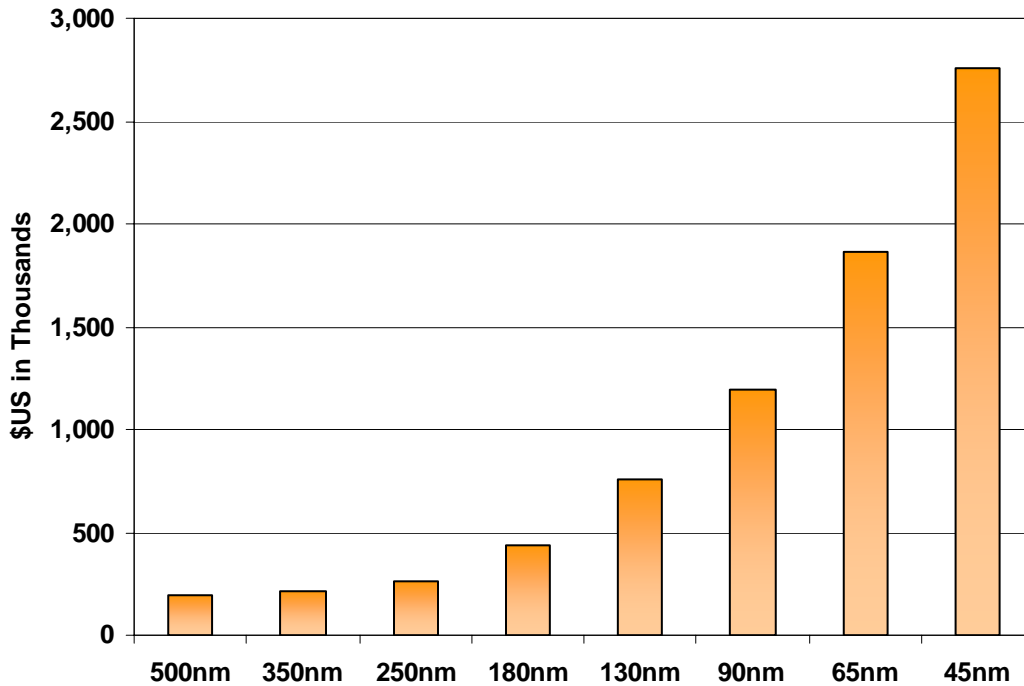
Figure 1. Exponentially Increasing Cost of Semiconductor Fab Capacity



Source: In-Stat, 1/07

Likewise, the cost of manufacturing continues to increase. The cost of developing mask sets, which are unique to every product, and usually every fab, exceeds US\$1 million per set at the 90nm process node and is expected to continue to increase exponentially with each future process node (Figure 2).

Figure 2. Exponentially Increasing Cost of Semiconductor Mask Sets



Source: In-Stat, 1/07

Now, the same exponentially increasing cost of building fab capacity and developing process technology is once again putting pressure on the market for change as the number of semiconductor companies with fabs and foundries continues to shrink to below 40. Many of the semiconductor manufacturers and foundries have turned to joint process technology development, which addresses one side of the cost equation. Chartered Semiconductor Manufacturing, IBM, and Samsung have now developed a new model that addresses both the process development and the end-to-end manufacturing capacity. The new model also provides for a new level of cooperation amongst all the ecosystem partners that extends to the providers of intellectual property (IP), Electronic Design Automation (EDA) tools, package and test capabilities, manufacturing libraries, manufacturing equipment, and even raw materials that all work toward a common set of design and manufacturing processes.

Evolution of the Semiconductor Business Model

The Old Model

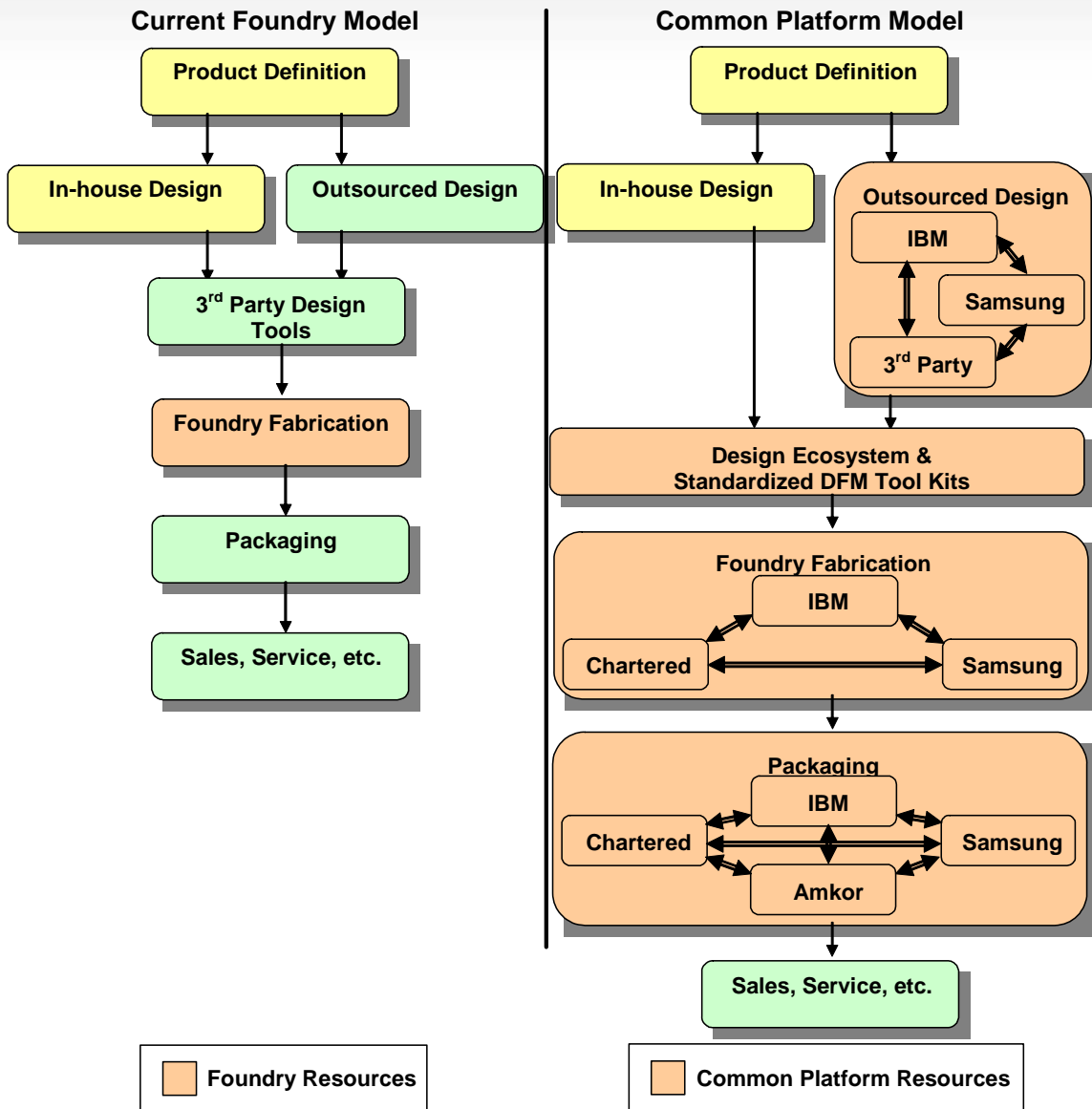
The birth of the semiconductor industry in the 1970s evolved around integrated design manufacturers (IDMs), which vertically integrated the entire semiconductor process, including design tools, design expertise, manufacturing processes, manufacturing capacity, sales and service. By the late-1970s, more specialized entities emerged that could more efficiently address various aspects of the value chain, such as distribution for sales and support. The manufacturing process, however, was a complicated aspect to outsource because of the relative infancy of the industry that was heavily reliant upon PCs for demand, customized tools and manufacturing process, and the efficiencies achieved through a vertically integrated design and manufacturing process. In the late 1980s, the semiconductor foundry business was formed by innovative Asian companies to provide a shared semiconductor manufacturing resource to smaller semiconductor companies. For an IDM, the foundry model involved the use of either in-house design resources or external design services followed by the choice of foundry and other supporting services, such as packaging (Figure 3). Another result was the development of an entirely new class of smaller innovative semiconductor design companies referred to as fabless that relied on the manufacturing expertise of the semiconductor foundries. Fabless companies now outnumber companies with 200mm or 300mm fabs by over 15:1.

The current model is now facing some of the same challenges of the IDM model with rising development costs of new process technology and manufacturing capacity. As a result, some foundries and IDMs have joined together in groups to jointly develop or license process technology to reduce the cost burden on one side of the equation. Unless the fabs of the various partners are synchronized, however, the client may not have the opportunity to utilize multiple manufacturers without additional costs of porting the products to each fab.

The New Model

Chartered, IBM and Samsung have developed a new foundry model for the semiconductor market that offers enhanced flexibility, portability, capacity, and resources. The new model is enabled by the Common Platform technology. The Common Platform technology collaboration is a working relationship between Chartered Semiconductor (further referred to as Chartered), IBM, and Samsung developed to implement a common process technology across all three companies. As shown in Figure 3, the new model provides a more vertically integrated approach similar to an IDM with the benefits of outsourcing services ranging from design through packaging.

Figure 3. Current and Common Platform Technology Foundry Models



Source: In-Stat, 1/07

The Common Platform technology relationship is the bulk Complementary Metal Oxide Semiconductor (CMOS) process technology that is jointly developed by IBM, Chartered, Samsung, and Infineon (note that Infineon is an IDM moving to a fabless model). The group began with joint development at the 90nm process node and has since extended the joint development to 65nm and 45nm processes. Although Samsung and Infineon joined the group after the 90nm process was developed, they have since licensed the 90nm process and collaborated in the joint development of 65 and 45nm nodes, which includes over 300 IBM process development engineers along with nearly 40 process engineers from each of the participating companies working together in Fishkill, New York.

Once the process is developed at IBM's Fab 323 in Fishkill, the process is rolled out to be qualified at fabs in IBM, Chartered and Samsung according to the schedules of each partner. At 65nm, there was significant overlap, and the technology qualifications at Chartered and Samsung were later than IBM by about 3 months. At 45nm, the qualifications will be simultaneous. The qualification and ramp process is coordinated by all partners who regularly share their insight and expertise. Throughout the ramp process, the performance of test chip vehicles¹ is compared to ensure that all processes are achieving similar results. Electrical data on the test chip vehicles used to compare the results of the 65nm bulk CMOS process from Chartered's Fab 7, IBM's B323 fab, and Samsung's S1 fab shows that all three factories have attained nearly 100% Cpk² yield in the last four months. Results illustrate that performance specifications are well matched in the three factories. Once the fabs are in operation fabricating the same designs, performance on test and product vehicles are compared on a quarterly basis, to ensure synchronization of the fabs. The result is having three foundries that can act individually or as one. In the latest report on fab synchronization, all three factories are centered on all 65nm Low Power device parameters within less than 5% deviation.

The result is the combined state-of-the-art fab capacity of three leading semiconductor manufacturing companies. Of the top ten semiconductor foundries, only 4 have 300mm wafer capacity and are manufacturing on the 90nm process node (Table 1) allowing for the smaller die sizes and power efficiency required by the high-volume fabless semiconductor companies developing state-of-the-art products. Individually Chartered and IBM are within the top five foundries, but together they rank third in current revenues; combined with the potential revenues from Samsung's dedicated foundry capacity, the Common Platform technology would likely rank second.

Table 1. Top Ten Semiconductor Foundries by Revenue

| Ranking | Foundry | 300mm Fab | 90nm Process |
|---------|------------------|-----------|--------------|
| 1 | TSMC | X | X |
| 2 | UMC | | |
| 3 | Chartered | X | X |
| 4 | SMIC | X | X |
| 5 | IBM | X | X |
| 6 | MagnaChip | | |
| 7 | Vanguard | | |
| 8 | Dongbu | | |
| 9 | Hau Hing NEC | | |
| 10 | Jazz | | |
| | Samsung | X | X |

Source: In-Stat, 1/07

¹ Semiconductor products designed to assist in testing and coordinating the manufacturing processes at multiple fabs.

² Cpk is a statistical measure of process consistency to specifications, of a plethora of electrical parameters across the three factories.

The Client Value Proposition

Individually, all three companies offer customers a legacy of engineering expertise and state-of-the-art manufacturing capacity, but as part of the Common Platform technology, the group offers much more. Each company has key strengths in different areas as summarized in Table 2, but the Common Platform technology collaboration brings together all the expertise and resources of each company into a unique entity that can take many forms depending on customer demands.

Table 2. Key Expertise of Common Platform Technology Partners

| | Chartered | IBM | Samsung |
|------------------------------|-----------|-----|---------|
| In-house product design | | X | X |
| Extensive product portfolio | | X | X |
| Extensive semiconductor IP | X | X | X |
| Design engineering services | | X | X |
| Advanced process development | X | X | X |
| Library & tool development | | X | X |
| Mask development | | X | X |
| 300mm manufacturing | X | X | X |
| Package engineering | | X | X |
| Packaging services | | X | X |
| Pure play foundry services | X | | |
| System design expertise | | X | X |

Source: In-Stat, 1/07

In the development of the new Xbox 360 processor codenamed Xenon, Microsoft turned to IBM for both design and manufacturing. According to Bill Adamec, Director of the Xbox Semiconductor Technology Group at Microsoft, the Common Platform technology was a factor in choosing IBM because of the potential for a quick ramp in demand for a new game console. Supporting the program required ramping the 90nm process at the IBM and Chartered fabs simultaneously, as well as packaging at Amkor, which also installed new capacity to support the program. According to Chartered, the ramp of the process technology was its fastest ramp to date, demonstrating the benefit of ramping a technology that had been developed and qualified at IBM's fab 323 nine months earlier. Despite some initial struggles in ramping production of the processor, having the two fabs and engineering teams to solve the manufacturing issues plus early qualification of a single packaging solution resulted in reducing the time-to-market of the processor and enabling Microsoft release the Xbox 360 on schedule.

Manufacturing Capacity and Efficiency

The Common Platform technology collaboration was formed on a key transition point for the industry—300mm wafers. This is a boundary that precludes many smaller players from entering or continuing in the manufacturing realm, but provides a significant increase in capacity for those that can. Just the use of 300mm wafers provides an average increase of 2.5X in volume of chips per wafer. Only 21 companies have announced plans to build 300mm fabs and of the 18 in operation, the combined manufacturing capacity of the Common Platform technology partners with the current fabs fully ramped represents 22% of total capacity and 60% of foundry-only capacity. In addition, both Chartered and Samsung have indicated that they are considering further expansions of their existing 300mm fabs to 70K wafers/month and/or the construction of additional fabs in the future. With three or more new 300mm fabs, which have an average life of three process generations, as the foundation, the large investment in the Common Platform technology ensures a strong and long-term commitment. Table 3 provides a summary of the fabs dedicated to the Common Platform technology.

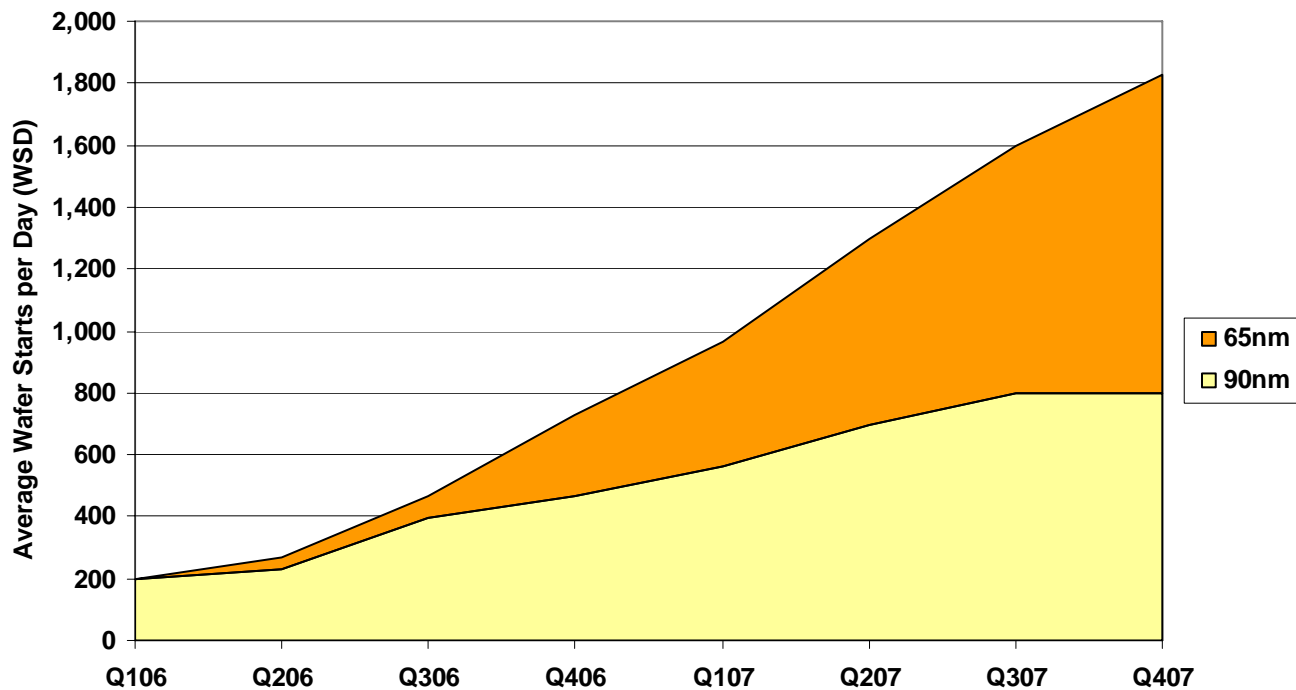
Table 3. Common Platform Technology Fabs

| Company | Fab | Location | Wafer Size | Installed Processes | Cleanroom Size | Capacity | Automation Tools | Key Technologies |
|-----------|---------|-------------|------------|---------------------|----------------|------------------|------------------|--|
| Chartered | Fab 7 | Singapore | 300mm | 90/65/45nm | 210k sq/ft | 30k wafers/month | SiView | Strained silicon, low-k, copper interconnects, SOI |
| IBM | Fab 323 | U.S. | 300mm | 90/65/45nm | 140k sq/ft | 15k wafers/month | SiView | Strained silicon, low-k, copper interconnects, SOI |
| Samsung | Fab S1 | South Korea | 300mm | 90/65/45nm | 175k sq/ft | 45k wafers/month | Proprietary | Strained silicon, low-k, copper interconnects |

Source: Chartered, IBM, and Samsung, 1/07

The fact that the three entities are all focused on continuously improving yields has led to improved fab efficiency at all three foundry partners. IBM and Chartered have already benefited from the relationship through the development of an advanced set of technology elements at the 90nm node and all three companies are reaping the benefits from this learning at 65 and 45nm nodes. Although Samsung has dedicated the S1 Fab to the Common Platform technology, Samsung continues to invest in additional 300mm fab capacity for its other semiconductor product lines, which could potentially be used for foundry purposes if necessary. Figure 4 illustrates the current planned capacity for the Common Platform technology at the 90nm and 65nm process nodes. For the client, the current and potential capacity at three companies translates into quicker time-to-market, higher delivery reliability, and greater elasticity to handle demand swings.

Figure 4. Common Platform Technology Capacity Plans Through 2007



Source: Chartered, IBM, & Samsung, 1/07

Manufacturing Flexibility

As a manufacturing agreement, one of the key benefits that the Common Platform technology manufacturing partnership offers foundry customers is flexibility. Customers can utilize one or multiple partners for manufacturing purposes that offer not only multiple fabs, but fabs that are geographically diverse. Thus, semiconductor designs

can be produced in different fabs for different customers or regions greatly reducing supply chain costs in a global environment. This model also mitigates economic or natural risks, which were not a concern in the early years of semiconductor manufacturing, but have become a critical concern as the industry has expanded globally, political environments have changed, and shocks have been experienced, such as the Great Hanshin Earthquake (often referred to as the Kobe earthquake) that struck Japan in 1995.

Unmatched Process Expertise

Although the Common Platform technology is aimed at semiconductor manufacturing, it is an extension of the IBM CMOS development alliance. Through its industry leading expertise in process technology and other relationships, IBM brings a wealth of knowledge and expertise to the development process. Overall, there are seven semiconductor foundries and IDM companies working on developing new process technologies together in Fishkill, New York, which is unmatched by any other development alliance or individual company. On August 29, 2006 the CMOS development alliance consisting of Chartered, IBM, Infineon, and Samsung announced the first circuits manufactured on a 45nm process and the availability of early design kits. The process will be one the first in the industry to use immersion³ lithography. Although the use of immersion lithography adds additional challenges to manufacturing, the 45nm CMOS process will be installed and qualified at Chartered, IBM, and Samsung by the end of 2007. Other semiconductor vendors, such as Intel, have indicated that they will not be using immersion lithography until a later process node, but that it will likely be required. The 45nm process development effort included 200 engineers from the four development partners with most collocated at the Fishkill location.

Increased Engineering Resources

Just as the global diversity of the manufacturing sites also mitigates risk, it also provides more manufacturing and engineering support. With the fabs located in Singapore, South Korea, and the East Coast of the United States, multiple engineering teams at multiple fabs can be working to resolve issues and improve manufacturing efficiency around the clock, rather than a single fab and engineering team in the traditional foundry model. With knowledge in different products, the Common Platform technology partners also offer a wide range of expertise and experience. This knowledge and support can be critical during the ramp of a new product. With three distinct companies joining together to coordinate yield ramps, various resources have been cross-geographically leveraged. Such resources include wafers and indigenous processes for yield learning and engineering talent and have led to cost reductions and industry-leading ramp times. In addition, when a change is introduced or one location experiences a problem, engineers from all three locations can work to resolve the issue and prevent the complete shutdown of individual or multiple lines. Such a scenario has occurred and will be highlighted in the Results in Action section. The result is a constant flow of information that has the potential to provide both current and future benefits to the fabless semiconductor customers.

Qualification and Packaging

The use of a common process technology and synchronized fabs allows for a single qualification for packaging even if multiple fabs are used in the manufacturing process. The synchronized fabs shared Graphic Data System II (GDSII) compatibility⁴. The result is that parts from one fab are identical to parts from other fabs. In addition, the close relationship of the partners throughout the product and process development process allows for early development and qualification of the packaging while reducing the risk of problems during the assembly process. The Common Platform technology offers a broad array of end-to-end packaging capabilities right to the module

³ The use of liquid materials to increase the optical resolution in the photolithography process.

⁴ GDSII is the industry standard database format for IC layout data exchange

level. IBM and Samsung have in-house capabilities, while IBM, Chartered and Samsung together have vendor partner capability through Amkor in Packaging, Assembly and Test (PAT). In terms of capacity, IBM and Samsung have some in-house capacity, while Amkor, the largest semiconductor packaging service provider, has 14 facilities worldwide, including three close to Samsung in South Korea and a new facility near Chartered's campus in Singapore.

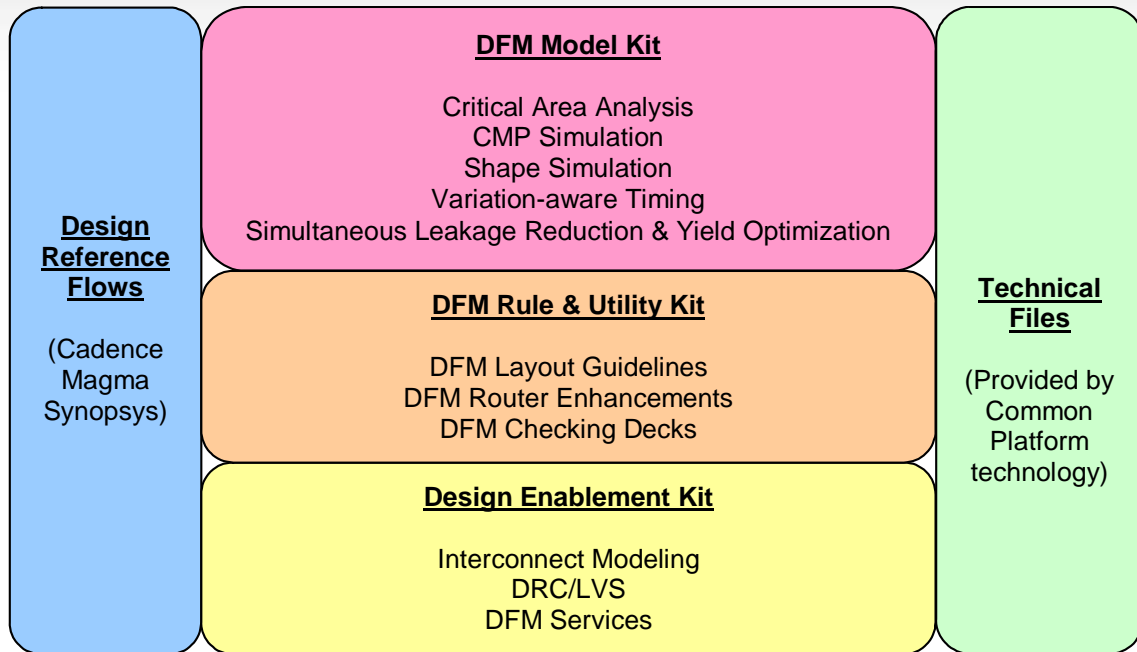
Common Resources

Another key advantage to the Common Platform technology is the common resources that are available, including Intellectual Property (IP), libraries, and tools. As IDMs, Samsung and IBM naturally have a considerable amount of IP available. Likewise, as foundries, Chartered and IBM have a considerable amount of licensable IP available. Since the processes and fabs are synchronized, once the IP is qualified at one fab, it is qualified for all of the fabs. In a similar manner, the Common Platform technology has licensed 3rd party libraries from both ARM (formerly Artisan) and Virage Logic for the 90nm process node and ARM for the 65nm and 45nm process node.

The importance of tight links between the EDA tool vendors and the technologies that are being used for chip design is becoming evident at 65nm. It is no longer acceptable to add margin to simple corner-based models and force designers to close timing, noise, power and yield targets by working around impossible guard bands. The Common Platform technology partners are including process and manufacturing data, not just to ensure good DFM practice, but also working with the leaders in the EDA industry to ensure that chip designers are able to understand the impact that subtle shifts in the process will have on their design's functionality and specs. This is achieved by all the partners working with Cadence, Magma, Synopsys and others, so that these effects can be modeled in an open fashion. Having reference flows from these companies that take into account the effects seen by the process experts is a requirement for anyone contemplating design at 65nm and beyond.

The final shared resource is tools. A critical attribute of the Common Platform technology is a common suite of 3rd party Design for Manufacturing (DFM) tools. The purpose of the DFM tools is to bring the critical aspects and considerations of the desired manufacturing process earlier into the planning and design process of the product. Using DFM allows designers to make decisions in the design that may affect various attributes of the product in manufacturing, such as power, thermal, timing, and signal integrity, as well as minimizing the die size and time-to-market. Achieving the desired cost, performance, and yields often requires trade-offs in many of these attributes. At the 90 and 65nm process nodes, the Common Platform technology offers a Design Enablement Kit and DFM Rule and Utility Kit, both designed jointly by the group (Figure 5). The kits provide design lines for developing products for the manufacturing process.

Figure 5. Common Platform Technology Design Tools and Resources



Source: IBM, 1/07

At the 65nm process node and beyond, The Common Platform technology collaboration goes a step further by recommending a suite of 3rd party tools called the DFM Model Kit that contains best-of-breed products available for every step in the design process (Table 4). Each tool was selected by a dedicated subcommittee formed to evaluate products in a specific area of manufacturing and/or product development. All the tools provide some level of modeling and simulation throughout the design process to allow the client to make the critical design decisions prior to taping out in silicon, which reduces the number of revisions, cost, and time-to-market. All of the kits and tools work with the design reference flows from Cadence, Magma, and Synopsys. The Common Platform technology also includes all the technical files required for use with each tool.

At the 65nm process node, at least one tool is selected for each aspect of the design process. The Common Platform technology has also announced early version of some of the tools for the 45nm process node, with the remaining tools available in early 2007. A continuous evaluation of the tools will occur at each process node to ensure that the best resources are available and that a common set of tools is recommended. Although specific tools are selected, the evaluation process has aided in establishing close relationships with all of the tool vendors while providing recommendations of future features and enhancements. The fabless semiconductor customer and EDA ecosystem should see significant benefits from the Common Platform technology efforts. In addition to the tools, IBM, Chartered and Samsung offer custom DFM services.

Table 4. DFM Model Tools and Suppliers

| DFM Function | Tool Supplier(s) | Description |
|------------------------|----------------------------|--|
| Design Guidelines | Common Platform Technology | Design guidelines jointly developed by Chartered, IBM, and Samsung |
| Checking Decks | Mentor | Priority rules compliance checking binned by criticality and relative yield |
| Reference Flows | Cadence, Magma, Synopsis | Place-and-route reference flows |
| Critical Area Analysis | Ponte | Identifies potential hotpots and susceptibility to manufacturing yield detractors |
| Lithography Simulation | Blaze | Simultaneous leakage reduction and yield optimization through timing-aware poly biasing |
| Lithography Simulation | Clearshape | Chip-level hotspot detection for shorts and other irregularities using shape simulation |
| Lithography Simulation | Mentor | IP-, cell-, and block-level litho simulation to allow for validation of the drawn versus printed shapes and detect problems early in design flow |
| CMP Simulation | Cadence | Validating accuracy for application in intelligent metal fill and improve interconnect modeling |

Source: IBM, 1/07

Although utilizing the Common Platform technology for manufacturing does not preclude a fabless semiconductor vendor from using other resources than those recommended, having a common set of IP, libraries and tools that are optimized for the design and manufacturability of products can greatly reduce the development time, manufacturing ramp, and overall cost of the final product. Using the Common Platform technology resources also assures a customer that the three industry leaders have selected the best solutions and have the experience in design and manufacturing with those resources.

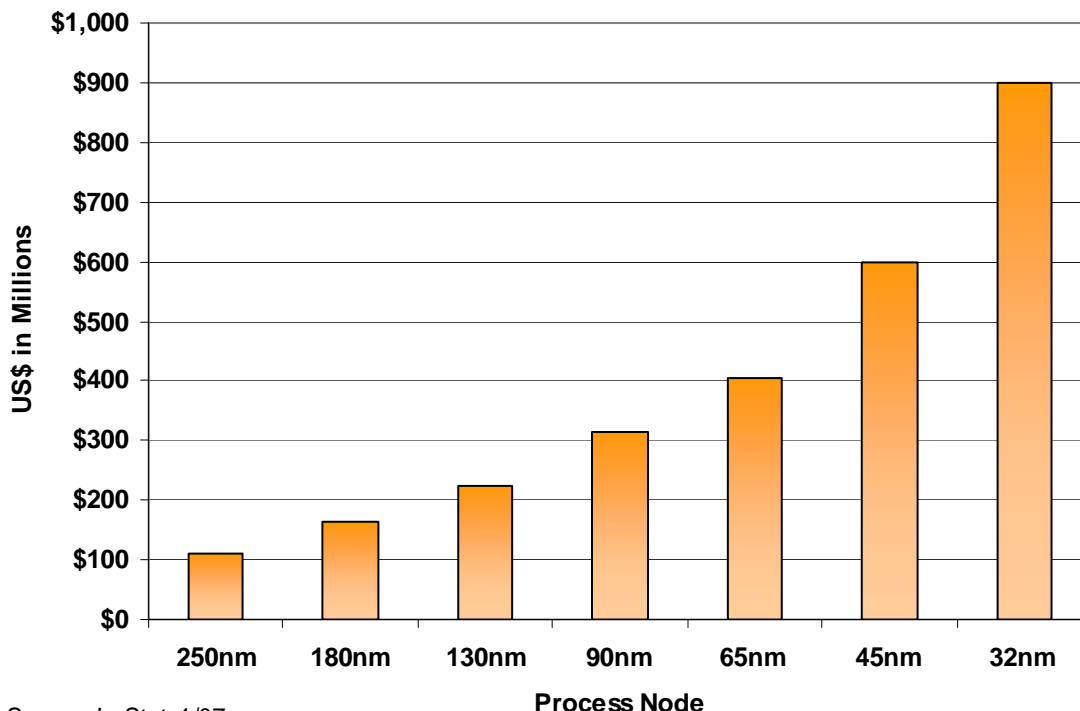
Ecosystem Development

In addition to the common design tools and resources, the benefits of the Common Platform technology extend to a much broader ecosystem that includes suppliers of manufacturing equipment, raw materials, and packaging by providing a common set of requirements for a large segment of the industry that are constantly evaluated and updated to improve the technology.

The Partner Value Proposition

The Common Platform technology formed by Chartered, IBM, and Samsung is an extension of the CMOS process development alliance, created for the purpose of sharing process development and ramping costs while providing joint manufacturing capabilities. Although the actual cost of developing a process node varies greatly from company to company, all semiconductor companies do agree that costs continue to escalate. Figure 6 demonstrates the average industry trend in process development costs for each process generation. TSMC indicated that developing its 90nm process was twice as expensive as the previous 0.13u process. As a result, TSMC is now licensing process technology in 65nm and possibly future advanced nodes from the Crolles2 process development alliance. On average, the cost of each process generation increases between 40%–50%, which results in an exponential trend.

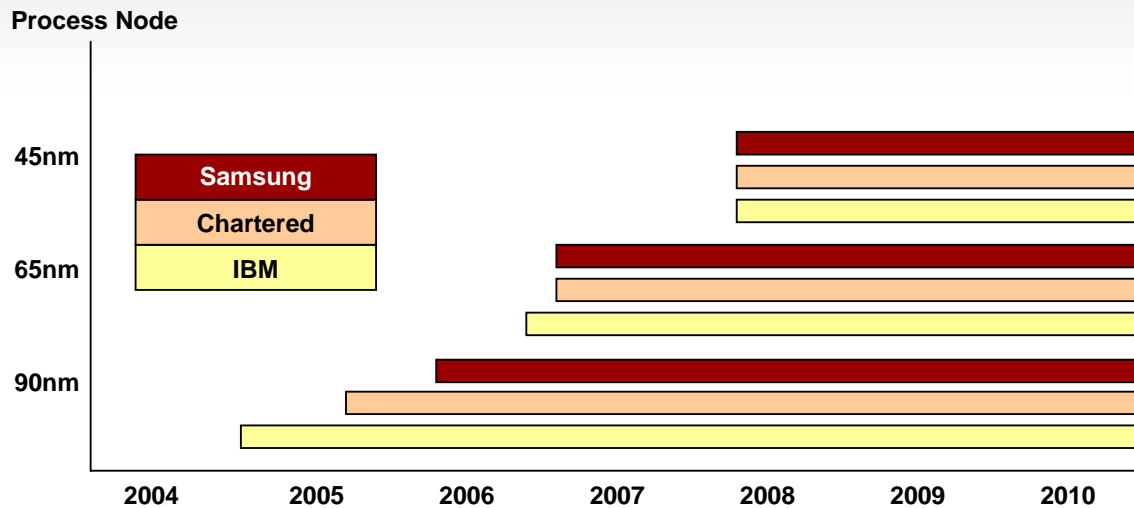
Figure 6. Average Development Cost Trend of Semiconductor Process Nodes



Source: In-Stat, 1/07

The partners with fabrication facilities, IBM, Chartered, and Samsung, have agreed to support the Common Platform technology on the 90nm, 65nm, and 45nm process nodes (Figure 7) for mainstream manufacturing. Discussions on future process nodes are underway. The 65nm low-power technology has been qualified at all three fabrication partners while 65nm standard foundry technology is currently being qualified for production beginning at all three companies by early-2007. The 45nm low-power technology will be installed and qualified at all three locations by the end of 2007 for production beginning in 2008.

Figure 7. Process Timeline and Roadmap



Source: Chartered, IBM, & Samsung, 1/07

In addition, each partner provides different benefits to customers of the Common Platform technology that, as a whole, are unmatched by any other single foundry.

Chartered Semiconductor Manufacturing

As one of the original and top three pure play semiconductor foundries, Chartered currently operates five fabs in Singapore, including four using 200mm wafers and one using 300mm wafers. The 300mm fab, Fab 7, was ramped using the first process jointly developed with IBM on the 90nm process node. Fab 7 will be ramping through 2007 with an anticipated capacity of 15,000 wafers/month by the end of 2006 and 30,000 wafers by the end of 2007 with a total clean room area of 210,000 square feet. Future fab expansions could increase this capacity even further. In addition, Chartered brings 13 years of foundry experience in manufacturing a variety of logic, memory, and RF components.

IBM

For over 40 years, IBM has been a leader in the electronics industry with solutions ranging from semiconductors to computing, networking, and printing solutions. In semiconductors, IBM is a leader in semiconductor process development and manufacturing with over 25 years of expertise and extensive intellectual property (IP) libraries. IBM has pioneered the industry transition to various process technologies, including copper interconnects, silicon-on-insulator (SOI), and low-k dielectrics. Although the Common Platform technology is based on CMOS technology, IBM also has manufacturing processes in SOI (developed in partnership with AMD, Toshiba, and Sony) and in Silicon Germanium.

IBM is also a leading provider of logic solutions ranging from its high-end Power series processors to its industry leading ASIC solutions. In addition, IBM has extensive design expertise and an intellectual property portfolio that extends to all types of semiconductor products. Going forward, IBM plans to concentrate on its system OEM business. With the potential for high volumes in communications and consumer applications, the Common Platform technology provides critical support for this strategy.

Samsung

Samsung is one of the largest high-tech conglomerates in the world with US\$52 billion in total annual revenues and \$18 billion in semiconductors alone. In addition to its leadership in many consumer electronics products and semiconductor memory, Samsung continues to expand its semiconductor product offering into other areas, such as embedded memory, application processors, wireless components and other sophisticated ICs. Samsung has 15 production facilities around the world and another fab under construction. The company also has five operating R&D lines. Semiconductor fabs are located in Giheung and Hwaseong in South Korea, and in Austin, Texas. IC assembly plants are operating in Onyang, South Korea and Suzhou, China. Samsung is the leader in 300mm wafer production, accounting for 31% of the total worldwide 12-inch wafer starts in 2005.

One 300mm fab, Fab S1, is dedicated to the Common Platform technology and foundry opportunities. Located on a 350-acre site in Giheung, Korea, the foundry was built in just 15 months and opened in May 2005. The fab is in production at 130nm and 90nm and will soon begin producing logic ICs using the jointly developed 65nm process. It has a round-the-clock staff that includes 400 engineers as well as dedicated resources for design, DFM, product engineering, test, failure analysis and reliability. Fab S1 has a total capacity of 45,000 300mm wafers/month with a total clean room area of 175,000 square feet.

Risk Mitigation

The three fabrication partners have inherent differences in goals from the alliance and distinct cultures and yet have embraced the complexity of synchronizing a single process across multiple fabs with due diligence. They are working to resolve geographical and equipment related differences. Thus far, however, Chartered, IBM, and Samsung have integrated their processes, teams and strategies efficiently.

Different Equipment and Fab Automation Tools

Companies with multiple fabs typically follow a copy-exact mantra to eliminate most factors that could introduce variances in the manufacturing process. As the largest semiconductor manufacturer in the world, Intel has almost perfected this effort, which often leaves the environmental conditions as the only potential issue. Although the Common Platform technology partners work together in evaluating equipment, the fab equipment is often different due to variances in time when the fabs are equipped, contractual agreements, and service and support from the equipment vendors. In addition, each company uses some elements of IBM's SiView fab automation tools, but each vendor customizes to its own requirements. The partners are working, however, to reduce the variance as much as possible. IBM's 323 Fab, Samsung's S1 Fab and Chartered's Fab 7 utilize approximately 70% of the same equipment including critical lithography systems. The existing differences do not pose risks with respect to process-matching. The differences between tools from various equipment vendors are, however, being reduced as more of the operational specifications are being driven by process development alliances, such as the two being led by IBM for bulk CMOS and SOI.

Different Mask Sets

Although the processes at each fab are GDSII compatible, each fab requires a different mask set for each product that is not compatible between fabs. This adds the cost of additional mask sets, which average over US\$1 million per chip for the 90nm process node. The use of different mask sets, however, mitigates schedule risk with the development of the masks and allows for easier debugging of masks if one set passes and another fails, as IBM and Chartered experienced with the first and second generation Xbox 360 processors. The additional cost of different mask sets, however, may be minimized by the internal mask development resources at IBM and Samsung. The cost may also be quickly offset by the rapid ramp in product volume at multiple fabs. Going forward, the Common Platform technology partners are working to use similar mask designs to collaborate on yield ramps and process integration.

Different Companies

The fact that each of the partners has a different business model adds a layer of complexity as well as versatility. IBM, who has been a leader in semiconductor process technology, has recently moved to a model that combines foundry manufacturing with ASIC and server development along with other engineering services. Chartered is a pure-play foundry, and it is continually expanding its expertise in process development, even solidifying a relationship with Amkor, a leading packaging company, after selling its Fab 1 building to Amkor for on-site package development and packaging services. Samsung, on the other hand, is one of the largest electronics conglomerates with significant success in Plasma TVs, LCDs, and cell phones over the past five years, in addition to its leadership position in semiconductor memory. Samsung has just recently announced offering engineering and logic foundry services.

Although the different goals of the companies would seem to be at odds, they are actually very symbiotic. Just as IBM looks to target high-volume applications, the company can use Chartered and Samsung for foundry resources in addition to its own capacity. In a similar manner, just as Chartered does not offer the product development engineering services, it can look to IBM and Samsung for that expertise. This also extends to the future strategies of each partner. Both IBM and Chartered admit that they could not have won the Microsoft Xbox 360 processor without their common manufacturing and fab ramp initiatives. Chartered could not have supplied the product development resources and IBM could not have supported the manufacturing requirements. Now other existing customers and partners of the Common Platform technology group are reaping the benefits as well.

Although the current agreement for the Common Platform technology extends through 2007, discussions are already ongoing for further extensions of this relationship. The high investment in process development; resources allocated to evaluate equipment, fab ramp and synchronization fabs efforts; and the benefits each partner stands to reap from the relationship provides strong justification for a long-term relationship. If anything, it increases the possibility of other partners in the future, a scenario that none of the existing partners will rule out.

Different Cultures

The cultural differences would appear to be by far the most challenging obstacle to overcome. Not only is each company located in a different region with a different culture and language, but each company is also a major competitor in their respective segments of the semiconductor market. Many of these barriers have been overcome with time and close working relationships. During the ramp of the 90nm process at Chartered and the ramp of the Xbox 360 processor, Chartered and IBM employees maintained continuous contact through on-site meetings, and rigorous use of test vehicles for synchronizing the performance of the fabs. Although Samsung entered the program at a later time, similar relationships have been developed as all three companies work jointly on a new product effort for QUALCOMM, a leader in communications technology. These close working relationships have also overcome delays customers would expect in dealing with more than one company by having project leads from each partner assisting in coordinating communications. Automated data sharing techniques are being set up between all three partners for continuous communication and troubleshooting. The presence of development engineering teams from all three companies in Fishkill, NY provides a great melting pot for assimilating cultural differences and focusing on the broader common goal of winning in the marketplace.

New Process Technologies

The introduction of new technologies in a manufacturing process, whether at a major process node or during the life of a process node, can always be disruptive, especially when multiple companies and fabs are involved. The use of multiple fabs, however, allows the changes to be introduced and tested without the risk of drastically altering the product of production flow before all potential problems are resolved. The Common Platform technology also provides the resources of several diverse engineering groups to resolve any issues that may arise.

The Common Platform technology is facing a major change in process technology at the 45nm process node with the introduction of immersion lithography. The new lithography process will require changes in process flow and material handling, and a potential increase in the overall process time. The three companies are working to ensure a quick transition and optimization of the process. In addition, being first to use immersion will provide the Common Platform technology partners and its customers with a competitive advantage over other semiconductor manufacturers and foundries.

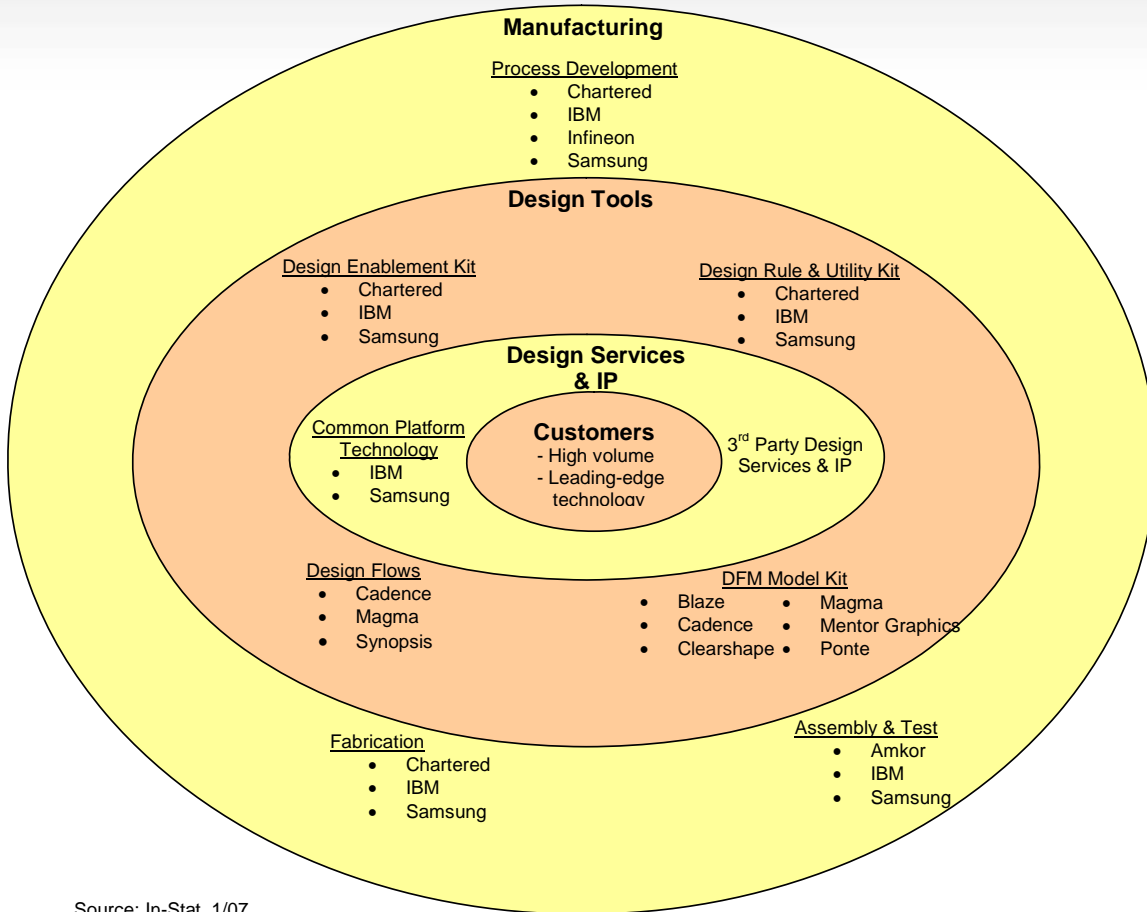
Results in Action

The partners in the Common Platform technology have indicated that they are working with several potential customers. Microsoft was a great proof point of joint development, qualification, process transfer, yield ramp and manufacturing between Chartered and IBM. Microsoft benefited significantly from the use of multiple fabs and multiple engineering teams. At least two other leading technology companies including Infineon and QUALCOMM are already seeing the benefits of the Common Platform technology initiative. Infineon has developed prototypes at IBM's East Fishkill facility using both the 90nm and 65nm common platform technology subsequently ramping production volumes with Chartered as a foundry source. QUALCOMM, which just recently announced that it will be using the Common Platform technology partners for its next generation cellular processor, will benefit from a mature learning curve, quick ramps, and the ability to leverage significant capacity upside generated by sourcing with IBM, Chartered, and Samsung.

Other clients of the individual Common Platform technology partners, such as AMD and its newly acquired ATI group, are likely to benefit from the ability to tap into technology leadership, multiple partner engineering synergies, and a multi-sourcing experience in much the same manner as did Microsoft. Not only is AMD using Chartered's Fab 7 for additional processor manufacturing, but AMD is also using an SOI process, similar to what was used for the Microsoft processor.

Just analyzing the alliances that each company has developed combined with the foundry customer base that Chartered and IBM, the fourth and fifth largest foundries by revenue in 2005, also bring to the table, it's clear that the Common Platform technology is as much an ecosystem generator as a manufacturing alliance as shown in Figure 6. Although the fabless semiconductor companies with high volumes, such as QUALCOMM, Broadcom, NVIDIA, ATI Technologies (now a division of AMD), and Xilinx, would experience significant benefits from the Common Platform technology, the rich design/EDA ecosystem generated by the relationships of all the parties involved is likely to equally benefit smaller fabless semiconductor companies.

Figure 8. The Ecosystem Around the Common Platform Technology



Source: In-Stat, 1/07

A Leading Industry Trend

There have been other industry alliances formed over the past few years to address some of the same issues with process development, including the Crolles2 Alliance and the Advanced SoC Platform Corporation (ASPLA). The Crolles 2 Alliance was formed in 2002 between STMicroelectronics, Philips Semiconductor, and Motorola (now Freescale). TSMC has since joined the alliance as a licensee. The alliance was formed to develop a joint 90nm process technology and has since been extended through the 32nm process node. In addition, the alliance has a pilot line in Crolles, just outside of Grenoble, France. At this point, the alliance is focused solely on the joint development of process technology, but the inclusion of TSMC adds a foundry component to the alliance that may be a way for the other members to extend their own manufacturing capabilities.

The ASPLA was formed in 2002 by eleven Japanese IDMs to jointly develop process technology at 90nm and beyond. The ASPLA includes Fujitsu, Hitachi, Matsushita, Mitsubishi, NEC, Toshiba, Oki, ROHM, Sanyo, Sharp, and Sony. Note that Toshiba and Sony are also in IBM's SOI development alliance. Now a smaller group including Fujitsu, NEC, Renesas, and Toshiba are considering jointly developing a 45nm process technology and the possibility of synchronizing fabs in a similar manner as the Common Platform technology partners. The partners in the Japanese group, however, are primarily IDMs, with most of their current resources located in the same region.

The formation of the IBM and other alliances signals a clear trend toward fewer processes as the cost escalates and the sharing of development resources, IP, and even manufacturing capacity increases in the future. Of the top ten semiconductor manufacturers in the world Intel (1) and Texas Instruments (3) are the only companies not involved in a process development alliance.

Conclusions

With the formation of several major technology alliances aimed at developing future process technology, there is a clear trend toward the co-mingling of development resources that are becoming part of the new semiconductor business model. Chartered, IBM, and Samsung have accomplished what would have seemed impossible a decade ago because of the difficulty with combining the resources of three companies with different products, market strategies, and cultures and extending the development model to include joint manufacturing capabilities. However, necessity driven by increasing development and manufacturing costs has proven to be a catalyst for industry change once again.

The Common Platform technology alliance has generated a number of new benefits to foundry customers, including:

- Full product development, manufacturing, and product lifecycle support from three leaders in semiconductor design, process technology, manufacturing, and assembly and test
- Multi-sourcing a single design through GDSII compatibility and globally-diverse synchronized fabs for risk mitigation and/or upside support
- Choice of design enablement resources (libraries, IP, reference flows, and EDA tools), including a robust set of Design for Manufacturing (DFM) tools jointly supported by multiple tool vendors, design centers, and foundry partners
- Engineering services and support from three companies with expertise in every aspect of semiconductor design and manufacturing

This new model is gaining tremendous momentum with two publicly announced high volume multi-sourcing clients, as least fourteen design tool/EDA/IP partners joining to provide a comprehensive design ecosystem plus the industry leading packaging vendor, Amkor. Microsoft was a powerful proof point to demonstrate IBM and Chartered's fab synchronization and manufacturing capabilities. Subsequent to that, QUALCOMM has now begun to leverage the platform's benefits announcing 90nm manufacturing. In the latest report on fab synchronization, all three factories are centered on all 65nm Low Power device parameters within less than 5% deviation. The Common Platform technology also has a strong roadmap for future technology development and capacity expansion.

List of Tables

| | | |
|----------|--|----|
| Table 1. | Top Ten Semiconductor Foundries by Revenue | 7 |
| Table 2. | Key Expertise of Common Platform Technology Partners | 8 |
| Table 3. | Common Platform Technology Fabs | 9 |
| Table 4. | DFM Model Tools and Suppliers..... | 13 |

List of Figures

| | | |
|-----------|--|----|
| Figure 1. | Exponentially Increasing Cost of Semiconductor Fab Capacity | 3 |
| Figure 2. | Exponentially Increasing Cost of Semiconductor Mask Sets..... | 4 |
| Figure 3. | Current and Common Platform Technology Foundry Models | 6 |
| Figure 4. | Common Platform Technology Capacity Plans Through 2007..... | 9 |
| Figure 5. | Common Platform Technology Design Tools and Resources..... | 12 |
| Figure 6. | Average Development Cost Trend of Semiconductor Process Nodes..... | 14 |
| Figure 7. | Process Timeline and Roadmap..... | 15 |
| Figure 8. | The Ecosystem Around the Common Platform Technology..... | 20 |

[Return to Table of Contents](#)

Offices

North America

Arizona
+1.480.483.4440

California
+1.408.243.8838

Massachusetts
+1.401.315.0613

Asia/Pacific

Singapore
+65 6780 4321

China
+86 10 6642 1812

Europe/Middle East/Africa

England
+44 (0) 1462 677062

Copyright In-Stat 2007. All rights reserved.

Reproduction in whole or in part is prohibited without written permission from In-Stat.

This report is the property of In-Stat and is made available to a restricted number of clients only upon these terms and conditions. The contents of this report represent the interpretation and analysis of statistics and information that is either generally available to the public or released by responsible agencies or individuals. The information contained in this report is believed to be reliable but is not guaranteed as to its accuracy or completeness. In-Stat reserves all rights herein. Reproduction or disclosure in whole or in part to parties other than the In-Stat client who is the original subscriber to this report is permitted only with the written and express consent of In-Stat. This report shall be treated at all times as a confidential and proprietary document for internal use only. In-Stat reserves the right to cancel your subscription or contract in full if its information is copied or distributed to other divisions of the subscribing company without the written approval of In-Stat.