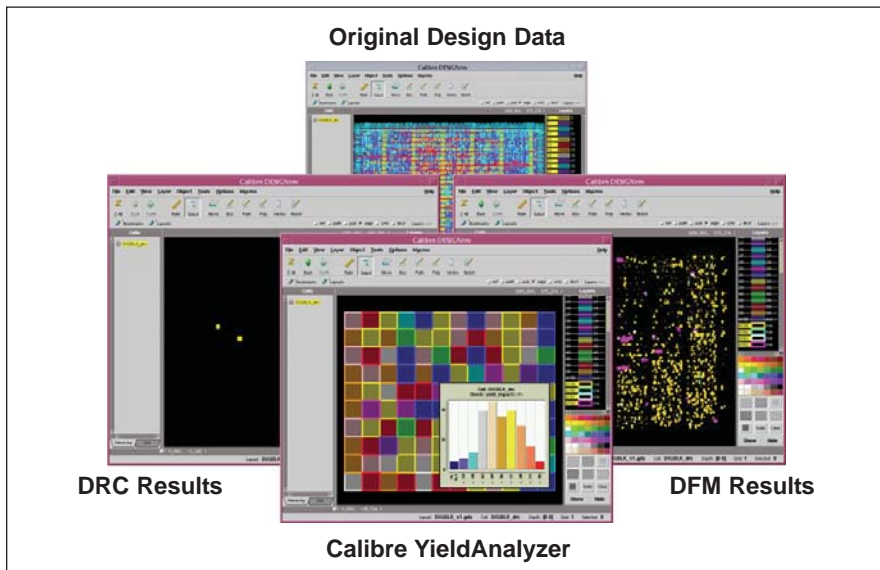


Calibre YieldAnalyzer

D A T A S H E E T



When a designer runs design rule checks on original design data (A), the problem is simple (very few failures to fix (B), and the goal is clear (fix them all). When the same designer then runs the foundry's recommended rule checks or critical area analysis, the problem is overwhelming (tens of thousands of errors (C), and the goal is unclear (how many and which ones should be fixed). With Calibre YieldAnalyzer (D), recommended rule violations and critical areas can be mathematically weighted by yield impact information to prioritize and trade-off which issues have the biggest impact on chip yield. This information is presented to the designer in reports and graphs within the designer's layout environment to guide them in using their available time to maximize impact on yield.

Bridging the Manufacturing to Design Communication Gap

As minimum design dimensions begin to approach half of the wavelength of light being used to print them, mask and process techniques alone cannot guarantee yield. Now additional work and resources are being shifted into the design flow to help address yield issues.

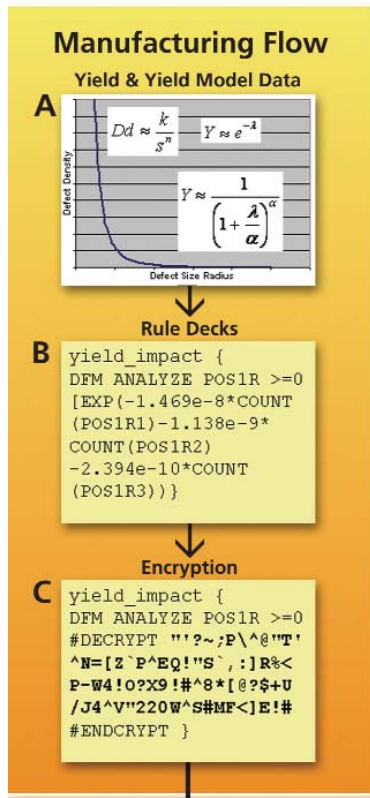
To effectively address these issues in design, manufacturing must be able to describe the layout features that interact with the process and communicate the amount of impact these features have on yield. Traditionally design rule decks have provided the means of communication from manufacturing to design, but yield impact is not a pass/fail metric as DRC is designed to communicate. There are complex mathematical models that relate the metrics of a particular design feature to its yield impact.

Calibre® YieldAnalyzer extends the SVRF language to support these complex mathematical models and feed the results to the Calibre RVE user interface for visualization and reporting within the design environment (ex. Calibre DESIGNrev). This helps the designer see through the fog of DFM rule violations and into the prioritized yield impact so that the most important issues can be addressed to maximize yield.

Key Product Benefits

- **Extends the traditional DRC language**, providing manufacturing teams a method of communicating yield and yield modeling information to the design teams.
- **Determines location of the most significant yield improvement opportunities** and provides graded yield metrics by issue, cell, window, etc.
- **Assesses the weighted “grayscale” of features** that fail to meet recommended rules.
- **Assesses the weighted sensitivity to random particles** using critical area analysis.
- **Evaluates both recommended rules and critical area analysis** in the same run deck and reviewing environment to understand trade-offs between types of analysis.
- **Runs analysis directly** on GDSII, OASIS, MilkyWay, and OpenAccess design databases.
- **Executes and visualizes analysis from within all the popular layout environments**, including Mentor Graphics IC Station and Calibre DESIGNrev, Cadence® Virtuoso/Encounter, Synopsys® Astro and Magma BlastFusion.
- **Extends the infrastructure for reporting and visualization** of these new statistical issues from within the design platform.

DFM Workflow for Calibre YieldAnalyzer



A Manufacturing determines yield and yield modeling information needed to communicate design to silicon interactions. This may include mathematical models that describe the variation in fail rates of recommended rules or defect densities distributions for particle shorts and opens.

B This information is codified into the rule decks using the SVRF and TVF language enhancements provided by YieldAnalyzer.

Mentor provides libraries of recommended rule analysis (RRA) and critical area analysis (CAA) templates that can be used to simplify the implementation.

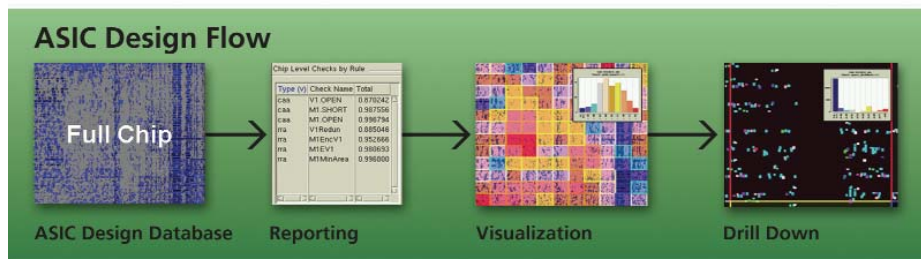
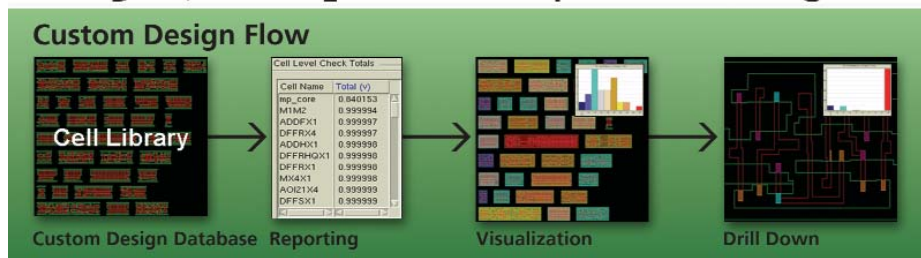
C Patented encryption technology can be applied to the decks to protect any sensitive intellectual property, yield models or specific yield weightings while still enabling the end user to run the analysis and measure the impact of design issues.

D Whether the design team is doing custom cell/block design or full ASIC chip design, the full complement of various RRA and CAA analyses can be applied.

E The analysis results can produce tabular reports without leaving the standard design tool environment to summarize the impacts by check or by cell to help determine the main yield detractors.

F These results can further be visualized in colormaps and histograms within the standard design tool environment to show the spatial variation of the worst impacting issues.

G Once the designer has determined the worst region of the worst impacting check, a drill down can be run to statistically weight individual occurrences of the issues within that region to further prioritize the worst impacting recommended rule violations or critical areas.



Through the variety of reports and visualizations the design team can determine the design practices or automated design tool behaviors that most impact the yield of their products so that informed trade-offs can be made regarding the various aspects of yield, area and performance.

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